REMARKS

The Examiner's Action mailed on October 4, 2006, has been received and its contents carefully considered.

Claims 1 and 9 are the independent claims, and claims 1, 3-6, 8, 9, 11-14 and 16 are pending in the application. For at least the following reasons, it is submitted that this application is in condition for allowance.

Claims 1, 3-6, 8, 9, 11-14 and 16 were rejected under 35 USC §103(a) as obvious solely over *Okada et al.* (US 6,093,243). This rejection is respectfully traversed.

An important object of the present invention is to control OFF-state leakage current and ON-state leakage current. This is described in page 12, lines 26-32 of the specification, for example:

> As described above, in the first embodiment, when a gate electrode is made of P^+-type polysilicon, a channel is N-type, the N-type impurity concentration in the channel is approximately 3×10^{17} cm^{-3}, a gate length is 0.15 μm, and a gate threshold voltage becomes 0.36 V. As a result, a normalized OFF-state leakage current I_{off}/W is reduced to a desired value, and too small ON-state current can be avoided.

To attain this object, the semiconductor device of the present invention must satisfy the following conditions (1) to (3), each of which is recited in both independent claims 1 and 9:

(1) the conductivity type of the gate electrode is P-type, and the conductivity type of the channel is N-type;

(2) the "impurity concentration in said channel is within a range approximately from 1×10^{17} cm^{-3} to 1×10^{18} cm^{-3}"; and

(3) "a channel length of said channel is within a range approximately from 0.1 μm to 0.25 μm".

There are two types of electrical charge carriers that move in the semiconductor layer, namely, electrons and holes in accordance with the conductivity types of the semiconductor layer. The speeds of movement of the electrons and the holes are different from each other.

Therefore, in the present invention, the object of which is to control OFF-state leakage current and ON-state leakage current that are equivalent to the movement of electrical charge carriers, the conductivity type of the semiconductor layer is an important condition for achieving the above object.

This is described in the specification, for example, in page 8, lines 7-10:

> As can be understood from the curve T0 in FIG. 3 indicating a case where the N-type impurity concentration in the channel is approximately zero, a gate threshold voltage is approximately 0.73 V when the gate length is approximately 0.4 μm or more.

Page 8, lines 26-29:

> As can be understood from FIG. 3, a gate threshold voltage can be decreased by increasing the N-type impurity concentration in the channel, that is, a gate threshold voltage can be adjusted by controlling the N-type impurity concentration in the channel.

And page 9, lines 7-10:

> In the first embodiment, since the gate electrode is made of P^+-type polysilicon, the channel of the SOI film 103 is N-type, and a gate threshold voltage is approximately 0.36 V, a normalized OFF-state leakage current I_{off}/W can be suppressed.

The Office Action alleges that *Okada et al.* discloses the overall structure of the claimed semiconductor devices, together with values of the impurity concentration in the channel region (6×10^{17} cm^{-3}) and of the channel length (0.25 μm) that fall within the claimed ranges, in one embodiment, and that *Okada et al.* discloses an SOI type FET in a different embodiment.

However, the Office Action admits that "*Okada et al.* does not disclose in the embodiment, an SOI type FET, and that said gate electrode is made of P-type and conductivity types of said source, said drain, and said channel are all N-type, rather discloses the impurity types are the other way around".

The Office Action states on the last line of page 2 thereof that to interchange the conductivity types in the device is obvious because they are recognized to be equivalent. However, since the speeds of movement of electrons and holes are different, the conductivity types are <u>not</u> equivalent when looked at from the viewpoint of the current flowing in the semiconductor layer.

As referred to above, Applicant has found that the effect of the present invention can be achieved by satisfying all of the above-mentioned conditions (1) to (3) . As *Okada et al.* does not employ the combination of a P-type gate electrode with an N-type channel, the desired effect would not be obtained. *Okada et al.* does not therefore teach or suggest "said gate electrode is made of P-type" as recited in claim 1 or "a gate electrode, which is made of P-type" as recited in claim 9, and nor does *Okada et al.* teach or suggest "conductivity types of said source, said drain, and said channel are all N-type" as recited in claim 1 or "conductivity types of the channel region, the source and the drain are all N-type" as recited in claim 9.

It is respectfully submitted that it would not have been obvious to have interchanged the impurity types of *Okada et al.* for the reasons given in the Office Action (that they are regarded as equivalent), because the difference in relative speeds of movement of the electrons in the N-type semiconductor material and of the holes in the P-type semiconductor material lead to unexpected advantages (reduction of leakage current) when a P-type gate and an N-type channel are combined with claimed features (2) and (3) of the invention as detailed above.

Accordingly, the presently claimed invention is novel and not obvious over *Okada et al.*, and claims 1 and 9 are allowable, together with all claims that depend therefrom.

It is submitted that this application is in condition for allowance. Such action and the passing of this case to issue are requested.

Should the Examiner feel that a conference would help to expedite the prosecution of this application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

Should any fee be required, however, the Commissioner is hereby authorized to charge the fee to our Deposit Account No. 18-0002, and advise us accordingly.

Respectfully submitted,

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Date

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